REMARKS

Summary Of The Office Action

Claims 10-19 were pending.

Claims 10-12, 14, 15 and 17 have been allowed. Further, the Examiner finds allowable subject matter in claims 13 and 16 and indicates that these claims also would be allowed if rewritten in suitable form.

Claim 18 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Desai et al. U.S. Patent No. 5,347,638 ("Desai"). Claim 19 has been rejected under 35 U.S.C. § 103(a) as being obvious over the Desai in view of Miller U.S. Patent No. 5,079,639. Claims 18 and 19 also have been rejected under 35 U.S.C. § 112 as being indefinite.

The Examiner has noted and objected to informalities in the Drawings, the Specification, and claims 13 and 16.

Applicants' Reply

Applicants also have amended the Drawings, and the Specification to remove the informalities that were kindly noted by the Examiner.

Applicants appreciate Examiner's finding of allowable subject matter in claims 10-17.

Applicants have amended claims 13 and 16, as suggested by the Examiner, to remove informalities. Accordingly, claims 13 and 16 should now be allowed.

Applicants traverse the rejections of claims 18 and 19.

Claims 18 and 19 have been amended to place the claim recitations in better US format. Applicant respectfully submits that the claims 18 and 19 now meet all § 112 requirements.

With respect to the prior art rejection, applicants' invention relates to arrangement and methods for efficient parallel processing or computing. As summarized in the Abstract of the Specification, the invention relates to methods and arrangements for instruction word generation for controlling of functional units inside a processor. The "execution or controlling" instructions words are generated "in-situ" by expanding or supplementing a "shortened" program word part with "previously used" strings of instruction word parts stored in a reference table. The reference table is indexed (e.g., by row) to allow for quick retrieval of the appropriate string of instruction word parts reused in generating a current "execution" instruction word.

Independent claim 18 is directed to an inventive arrangement, which is configured to generate "execution" instruction words by retrieving an appropriate row of instruction word parts from memory. Applicants note that Desai's apparatus is configured for reloading microinstruction code to an SCI sequencer. Desai does not disclose a buffer for storing previously-used instruction word parts or which is addressed to recall previously-used instruction word parts [for reuse in generating "new" instruction words for execution], as is required by claim 18. Therefore, claim 18 is patentable over Desai. Further, dependent claim 19 is patentable over the cited prior art for at least the same reason that parent 18 is patentable.

Conclusion

Applicants respectfully submit that this application is now in condition for allowance. If there are any remaining issues to be resolved, applicants respectfully request that the Examiner should kindly contact the undersigned attorney by telephone for resolution.

By: _____
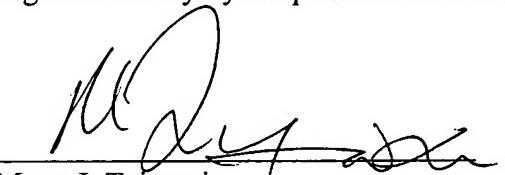
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Amendments to the Drawings

Applicants have amended FIG. 1 to show connections between Sequence Memory

9 and Pointer Registers 18 and 19. No new matter has been added.

Replacement drawings corresponding to FIGS. 1 and 2 are enclosed.

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